Merrick3 User Manual

Issue – 1.0

Kit Contents

You should receive the following items with your Merrick3 development kit:

1 - Merrick3 Board
2 - Programming Cable

Foreword

PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR MERRICK3 BOARD.
PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THIS MANUAL.

Trademarks

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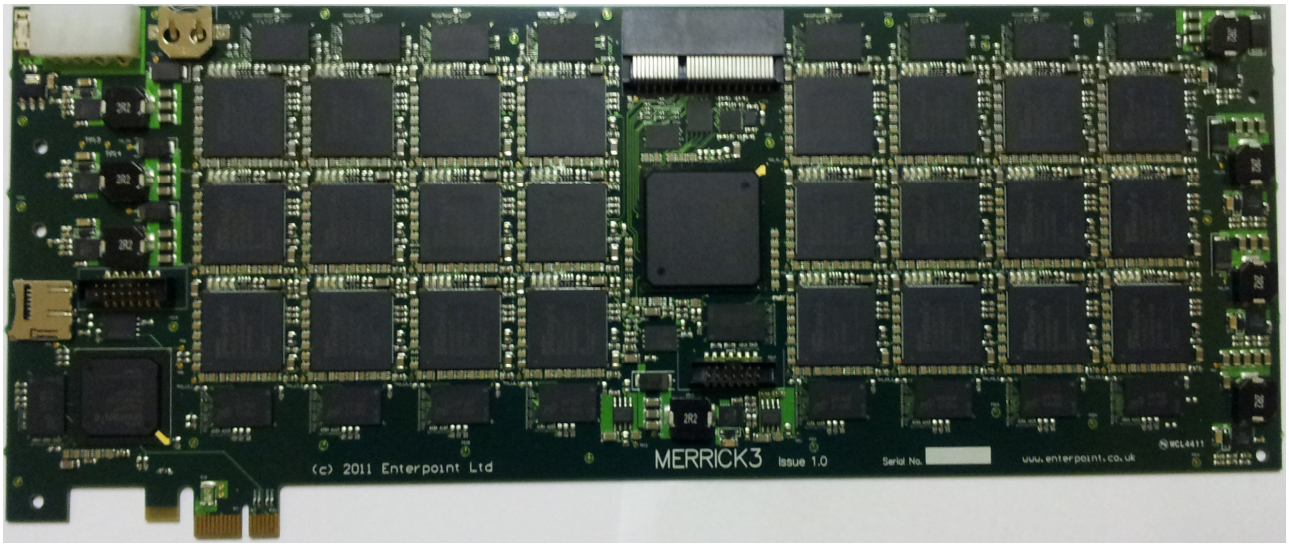
MERRICK3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Introduction

Welcome to your Merrick3 board. Merrick3 is a Spartan-6 based FPGA development board offering a highly powerful approach to prototyping FPGA and System designs.

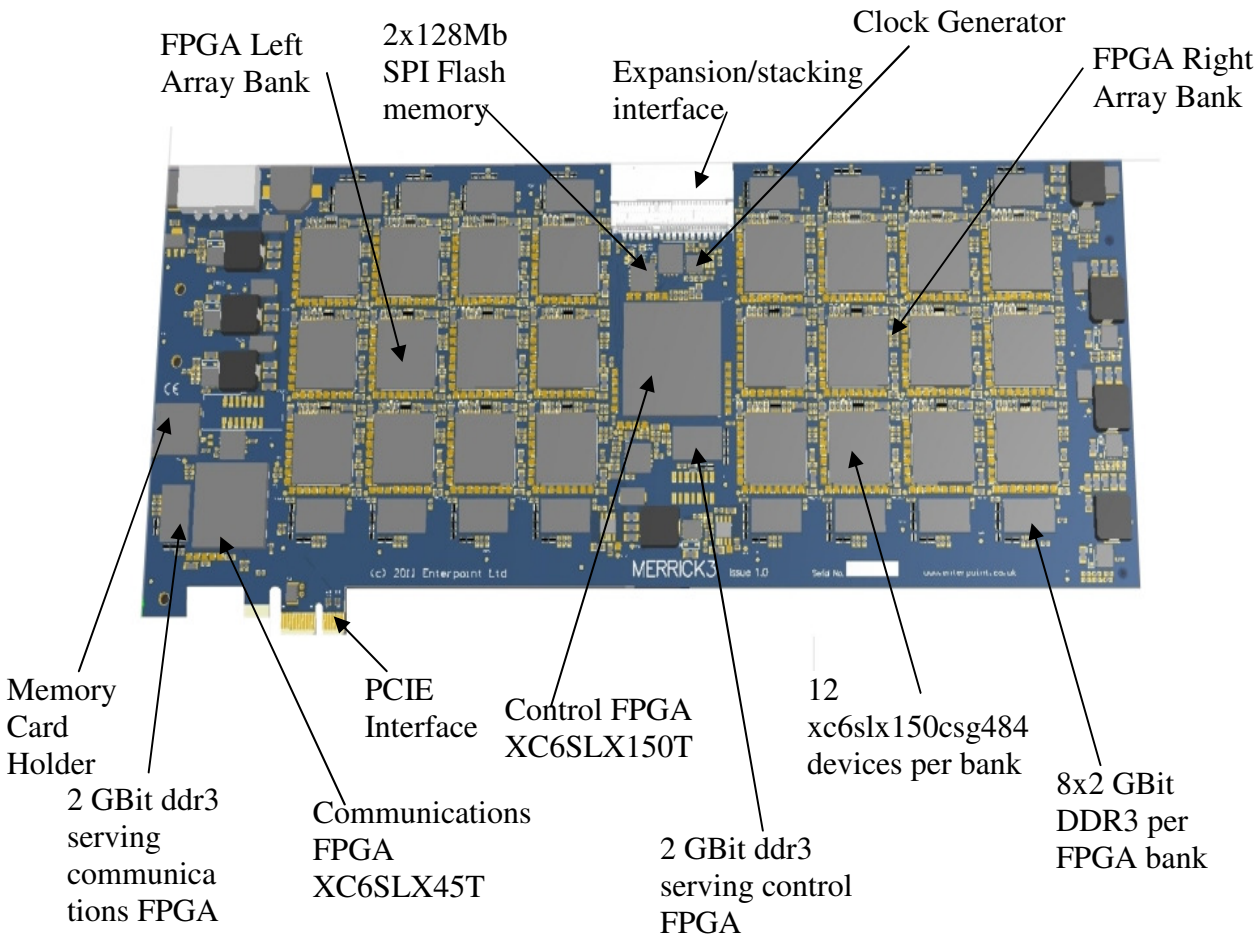
Merrick3 is a product for the high performance computing (HPC) marketplace. Based on an array of 24 XC6SLX150 FPGAs and 16 DDR3 this board delivers algorithm processing up to 10000X that of a X86 processor whilst operating with a power envelope of between 10-200W. In addition the board features high speed routing across the array and array reload (under 0.25 seconds), a board stacking interface and a PCI-E interface. We are also able to provide a separate algorithm implementation service for customers.

Merrick3 also offers a highly powerful approach to prototyping FPGA and System designs.

The aim of this manual is to assist in using the main features of Merrick3.
There are features that are beyond the scope of the manual. Should you need to use these features then please email support@enterpoint.co.uk for detailed instructions.

Merrick3 is currently fitted with XC6SLX150-2FGG484C Spartan-6 devices. Other variants may be offered at a later date or as an OEM product. Please contact us on boardsales@enterpoint.co.uk should you need further information.

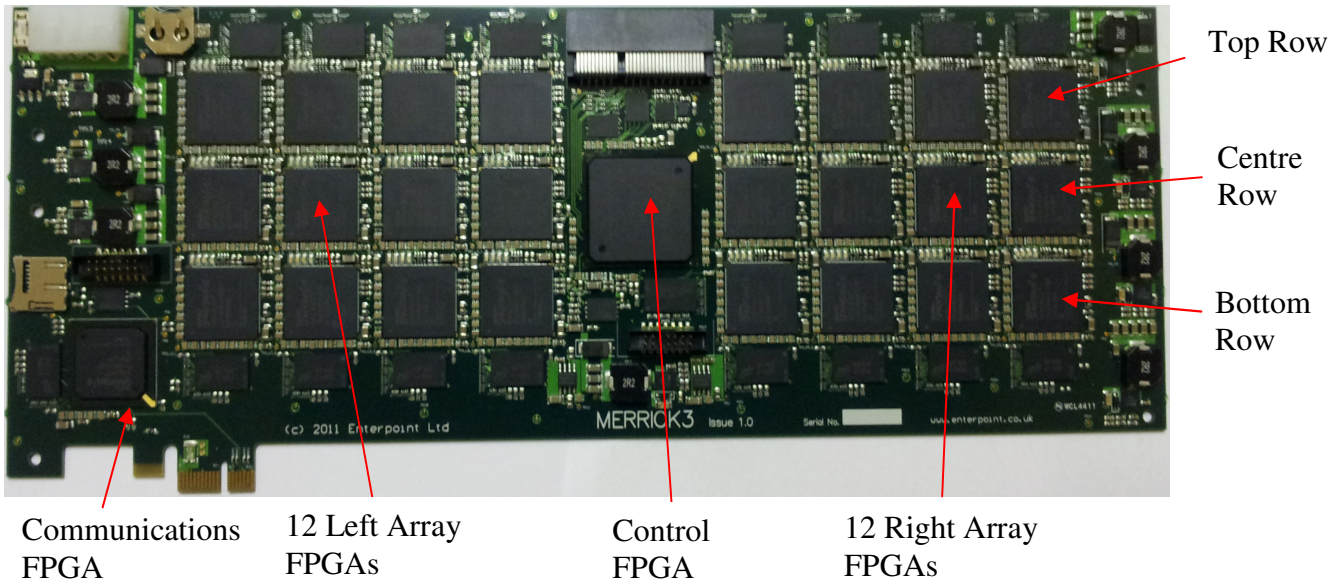
Merrick3 Features



Your Merrick3 will be supplied un-programmed. Unless you have bought an OEM product your board will be supplied with either a Prog2 parallel port programming cable or a Prog3 USB port programming cable.

The Spartan-6 FPGAs on the standard Merrick3 board are not supported by the free Webpack version of ISE. You will need version 11.1 SP4, or later, of the ISE tools, which are available from Xilinx at www.xilinx.com.

FPGAs



Merrick3 has a total of 26 FPGAs. There are 24 array FPGAs, one Control FPGA and one Communications FPGA. The standard arrangement is:

Communications FPGA – XC6SLX45T-FGG484C
Control FPGA – XC6SLX150T-FGG900C
Array FPGAs - XC6SLX150-CSG484C

Merrick3 is normally available with commercial grade -2 speed devices fitted in the XC6SLX150 size. Should you have an application that needs different size FPGAs, industrial specification parts or faster speed grades please contact us for a quote at boardsales@enterpoint.co.uk.

The Merrick3 FPGAs are highly interconnected. The diagram below shows the major sets of interconnections:

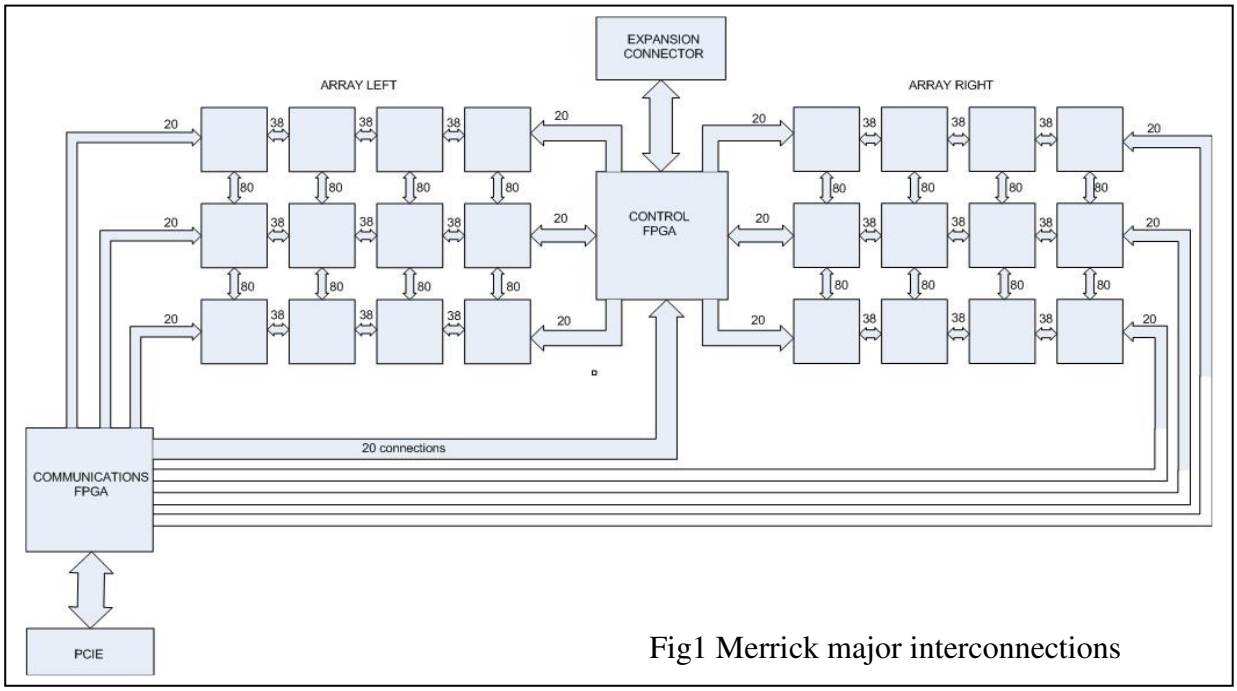


Fig1 Merrick major interconnections

CONNECTIONS BETWEEN FPGAs

1. Between Communications FPGA and Control FPGA

There are 20 connections between the Communications FPGA and the Control FPGA, arranged as 10 pairs between 3.3V IOs. The table below shows the pin connections:

SIGNAL NAME	COMMUNICATIONS FPGA	CONTROL FPGA
COMMS_BUS1	J3	V26
COMMS_BUS2	J1	V27
COMMS_BUS3	F3	R21
COMMS_BUS4	E4	R22
COMMS_BUS5	D2	R24
COMMS_BUS6	D1	R25
COMMS_BUS7	G3	T28
COMMS_BUS8	G1	T30
COMMS_BUS9	J4	U27
COMMS_BUS10	H3	U28
COMMS_BUS11	H2	U29
COMMS_BUS12	H1	U30
COMMS_BUS13	C1	R27
COMMS_BUS14	B1	R28
COMMS_BUS15	H4	T26
COMMS_BUS16	G4	T27
COMMS_BUS17	K2	Y24
COMMS_BUS18	K1	Y25
COMMS_BUS19	E3	T24
COMMS_BUS20	E1	T25

2. Between Control FPGA and Array FPGAs

There are a total of 4 sets of connections between the control FPGA and the array FPGAs.

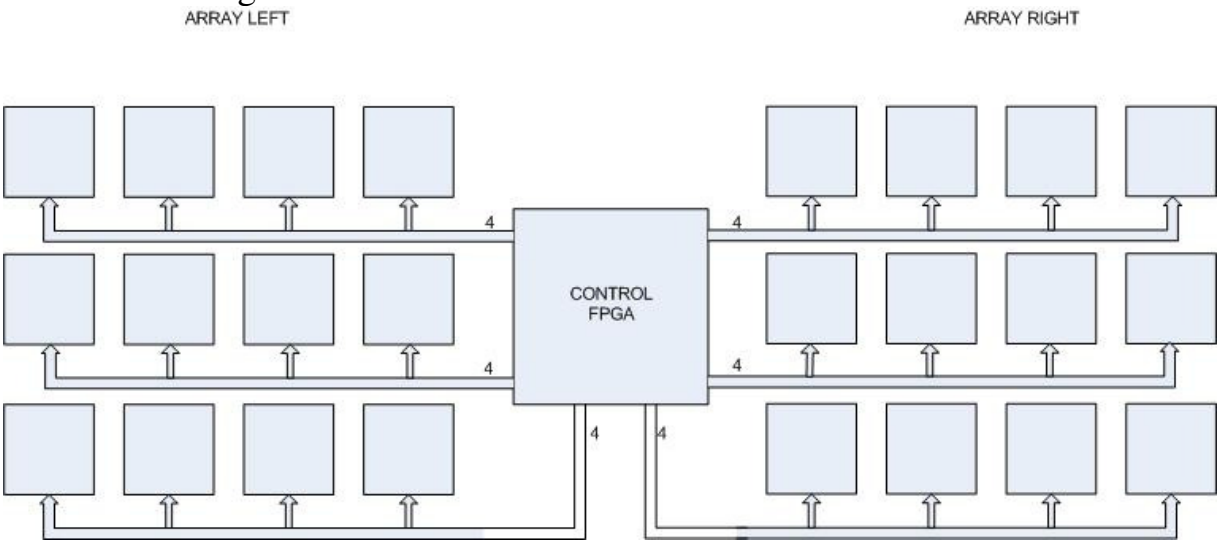
1. PATCH BUS SIGNALS

There are 120 connections shown in the diagram above (fig1) arranged as 20 signals (10 pairs) each to the nearest FPGA in each row. The connections are shown in the table below. In the schematics and .ucf file these connections are called, for example, PATCH_LH1BUS(1 to 20) for the 20 signals connected to the 20 RBUS signals on the top left row FPGA nearest to the Control FPGA and PATCH_RH3BUS(1 to 20) for the 20 signals. connected to the 20 LBUS signals on the bottom right row FPGA nearest to the Control FPGA. These connections are between IOs operating at 3.3V.

SIGNAL NUMBER	LEFT TOP ROW	LEFT CENTRE ROW	LEFT BOTTOM ROW	RIGHT TOP ROW	RIGHT CENTRE ROW	RIGHT BOTTOM ROW
1	AB10	AD12	AA19	D6	G14	G20
2	AB9	AE12	AB19	C6	F14	F20
3	AC11	AB14	AC19	E7	F15	K20
4	AD11	AC14	AD19	D7	E15	J20
5	AA11	AJ15	AD20	F8	B15	L21
6	AB11	AK15	AE20	E8	A15	K21
7	AE13	Y16	AB21	K10	H17	G22
8	AF13	AB16	AC21	J10	G17	F22
9	AC15	AJ17	AE23	L12	C16	J22
10	AD15	AK17	AF23	K12	A16	H22
11	AD14	AH16	AA22	H11	E16	F24
12	AE14	AK16	AC22	G11	D16	E24
13	Y15	AD18	AE24	M13	B17	D24
14	AA15	AE18	AF24	L13	A17	C24
15	AB17	AA18	AF25	J13	G18	B25
16	AD17	AB18	AG25	H13	F18	A25
17	AB13	AF16	AD22	J12	H16	F23
18	AC13	AG16	AE22	H12	G16	E23
19	AE17	W20	AD24	L14	L17	E25
20	AF17	Y20	AC24	K14	K17	D25

2. CLOCK SIGNALS

There are also 4 clock signals (2 pairs operating at 3.3v) which connect between the Control FPGA and global clock pins on the Array FPGAs. Each set of 4 clock signals is routed to a row of 4 FPGAs.



The connections to the array FPGAs are shown in the table below:

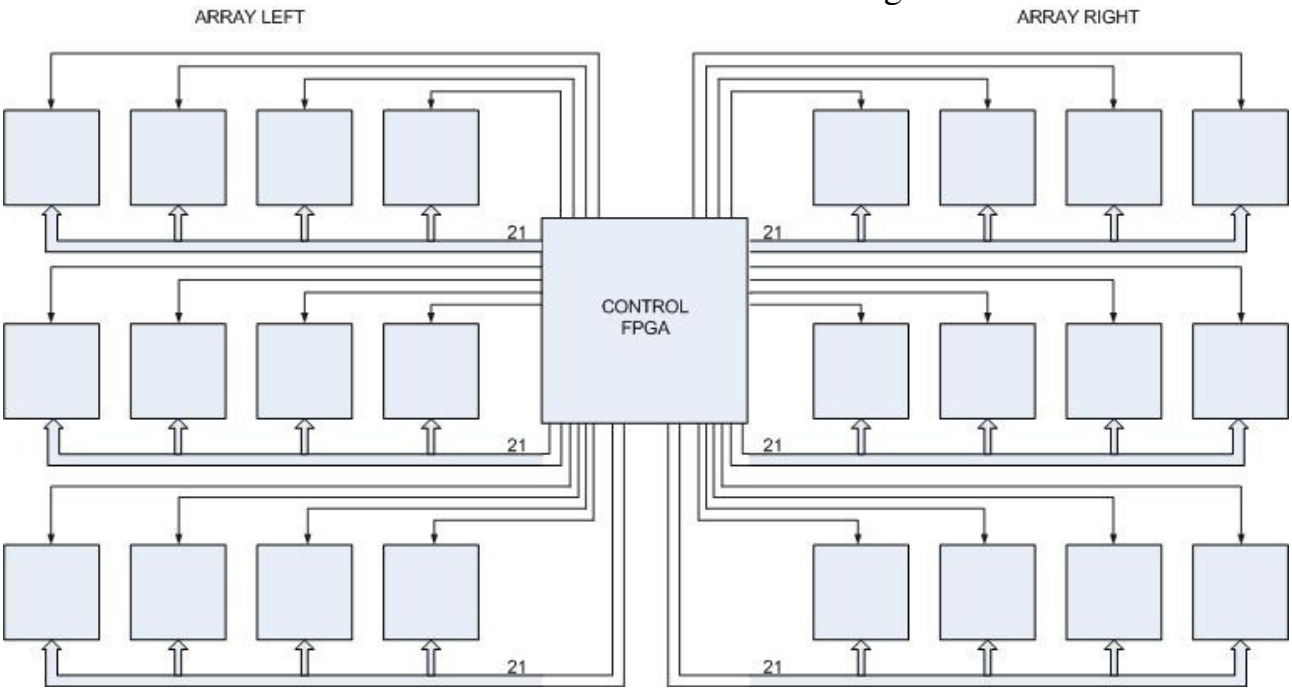
SIGNAL NAME	ARRAY FPGA PIN
CLK1	B10
CLK2	A10
CLK3	C11
CLK4	A11

The connections to the Control FPGA are shown in the table below. In the schematics and .ucf file these connections are called, for example, CLOCKS_LH1_(1 TO 4) for the 4 signals connected to the CLK(1 TO 4) signals on the four top left row FPGAS and CLOCK_RH3_(1 to 4) for the 4 signals connected to the CLK(1 TO 4) signals on the four bottom right row FPGAS.

ARRAY SIGNAL NAME	LEFT TOP ROW	LEFT CENTRE ROW	LEFT BOTTOM ROW	RIGHT TOP ROW	RIGHT CENTRE ROW	RIGHT BOTTOM ROW
CLK1	AC3	AD7	AC28	N5	T9	N27
CLK2	AC1	AE7	AC27	N4	T8	N28
CLK3	AB4	AB7	AE25	J5	P7	N29
CLK4	AB3	AB6	AE26	J4	P6	N30

3. CONFIGURATION SIGNALS

There are 23 configuration signals routed along each block of 4 FPGAs, with an individual Chip Select signal to each FPGA. This is to enable the Control FPGA to initiate reconfiguration of the array FPGAs. A 16 bit configuration data bus plus CCLK, PROGRAM_B, INIT_B, DONE and RDWR_B signals are connected to the Control FPGA as shown in the diagram below.



The connections to the Array FPGAs are shown in the table below:

SIGNAL NAME	ARRAY FPGA PIN	SIGNAL FUNCTION
CONFIG_DATA0	Y17	16 BIT CONFIGURATION DATA BIT 0
CONFIG_DATA1	V13	16 BIT CONFIGURATION DATA BIT 1
CONFIG_DATA2	W13	16 BIT CONFIGURATION DATA BIT 2
CONFIG_DATA3	AA8	16 BIT CONFIGURATION DATA BIT 3
CONFIG_DATA4	AB8	16 BIT CONFIGURATION DATA BIT 4
CONFIG_DATA5	W6	16 BIT CONFIGURATION DATA BIT 5
CONFIG_DATA6	Y6	16 BIT CONFIGURATION DATA BIT 6
CONFIG_DATA7	Y9	16 BIT CONFIGURATION DATA BIT 7
CONFIG_DATA8	AA6	16 BIT CONFIGURATION DATA BIT 8
CONFIG_DATA9	AB6	16 BIT CONFIGURATION DATA BIT 9
CONFIG_DATA10	V15	16 BIT CONFIGURATION DATA BIT 10
CONFIG_DATA11	W15	16 BIT CONFIGURATION DATA BIT 11
CONFIG_DATA12	Y16	16 BIT CONFIGURATION DATA BIT 12
CONFIG_DATA13	AA12	16 BIT CONFIGURATION DATA BIT 13
CONFIG_DATA14	Y11	16 BIT CONFIGURATION DATA BIT 14
CONFIG_DATA15	AB11	16 BIT CONFIGURATION DATA BIT 15
CONFIG_DATA16	AA1	PROG_B
CONFIG_DATA17	Y5	INIT_B
CONFIG_DATA18	U16	DONE
CONFIG_DATA19	W17	CCLK
CONFIG_DATA20	AB9	RDWR_B
CONFIG_DATA21	Y18	M0
CONFIG_DATA22	U15	M1

The connections to the Control FPGA are shown below:

CONFIG_ DATA SIGNAL	LEFT TOP ROW	LEFT CENTRE ROW	LEFT BOTTOM ROW	RIGHT TOP ROW	RIGHT CENTRE ROW	RIGHT BOTTOM ROW
0	N3	AK3	AG27	N1	E1	P22
1	AA5	AG5	AJ29	L1	B2	R30
2	R1	AE5	AJ30	K4	D2	U24
3	T2	Y8	AE30	H2	A5	W28
4	T3	AA10	AE28	H3	C4	V28
5	T1	Y9	AE29	H1	B5	W30
6	U1	W11	AA29	G4	C5	W27
7	AD3	AA9	AC29	J1	D4	P27
8	T6	W10	AA28	G1	E5	Y28
9	T4	Y11	AA27	G5	M7	P5
10	R3	AJ4	AH30	L4	M6	P28
11	AA4	AK5	AK29	L3	A2	R29
12	P1	AH5	AJ28	M1	C1	P24
13	R4	AF6	AF28	K3	A3	U25
14	R6	AD6	AD26	K2	D3	V24
15	R5	AE6	AF30	K1	B3	V23

16	V7	V9	AA24	F1	H6	Y26
17	U3	V10	AA25	G3	D5	Y30
18	P2	AH3	AK27	M2	D1	P30
19	P3	Y3	AH27	M3	E4	P23
20	R7	AC6	AE27	H4	A4	V30

The M0 and M1 signals for the left side array and right side array are routed independently. The table below shows the connections to the Control FPGA:

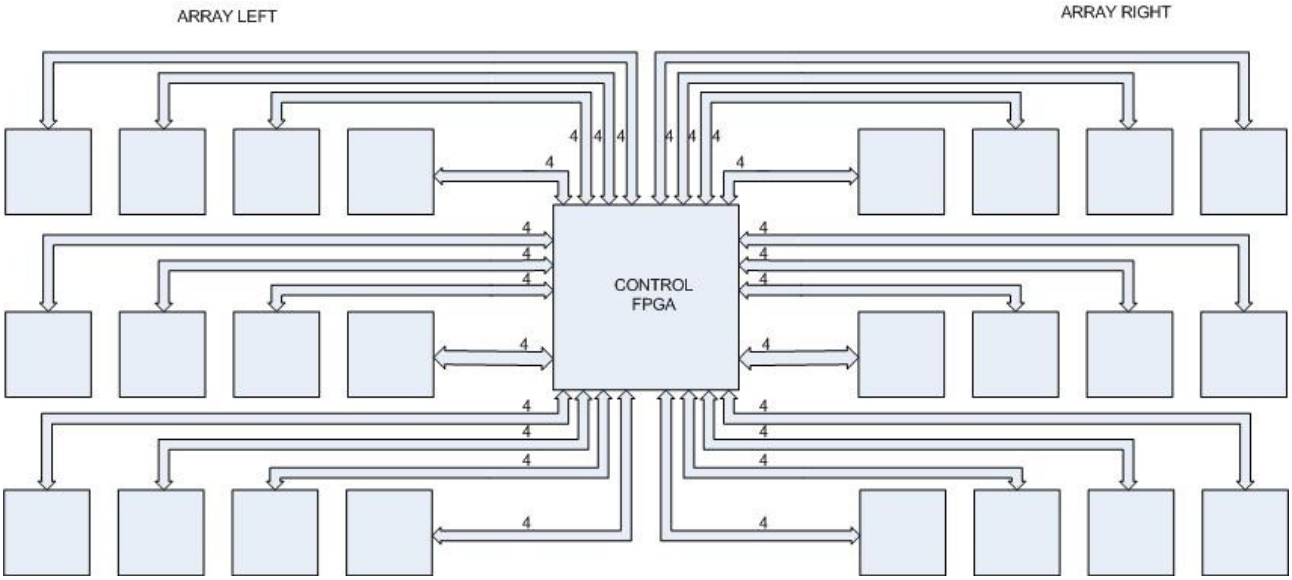
SIGNAL	LEFT ARRAY PIN	RIGHT ARRAY PIN
M0	W22	W21
M1	Y23	Y22

The individual Chip select pins, which connect to pin **AB5** of each array FPGA (CSO_B) are connected to the Control FPGA as follows, FPGA1 being nearest to the control FPGA and FPGA4 being furthest from the Control FPGA:

	FPGA1	FPGA2	FPGA3	FPGA4
LEFT TOP ROW	W3	W1	V8	U4
LEFT CENTRE ROW	AG29	W9	AH24	AG28
LEFT BOTTOM ROW	AD28	AD27	AD30	AA30
RIGHT TOP ROW	F4	F2	L6	F3
RIGHT CENTRE ROW	N9	N10	N8	J6
RIGHT BOTTOM ROW	Y27	AB28	AB30	AC30

4. INDIVIDUAL FPGA PATCH SIGNALS

Lastly there are 4 signals (2 pairs operating at 3.3V) which are routed to each individual FPGA from the Control FPGA.



The connections to the Array FPGAs are:

SIGNAL NAME	ARRAY FPGAS
PATCH1	D17
PATCH2	C16
PATCH3	B18
PATCH4	A18

The connections to the Control FPGA are shown below, FPGA1 being nearest to the control FPGA and FPGA4 being furthest from the Control FPGA. The signal names in the table below relate to the Array signal names in the table above. The schematic and .ucf file signal names take the form:

PatchAB_C_D where A = R(Right Array) or L(Left Array)
B = Row number = 1(top), 2(Centre) or 3(Bottom)
C= FPGA number 1 to 4
D = Patch signal number 1 to 4

So for example PATCHL1_3_4 connects to the PATCH4 signal on the 3rd FPGA in the top row of the left array.

SIGNAL NAME	LEFT TOP ROW			
	FPGA1	FPGA2	FPGA3	FPGA4
PATCH1	AH7	AG8	AE11	AG6
PATCH2	AK7	AH8	AF11	AH6
PATCH3	AD8	AF7	AE9	AD10
PATCH4	AE8	AG7	AF9	AE10
SIGNAL NAME	**LEFT CENTRE ROW**			
	FPGA1	**FPGA2**	**FPGA3**	**FPGA4**
PATCH1	AB12	W14	Y14	AC16
PATCH2	AC12	Y13	AA14	AD16
PATCH3	AC9	W12	Y17	AE15
PATCH4	AD9	Y12	AA17	AF15
SIGNAL NAME	**LEFT BOTTOM ROW**			
	FPGA1	**FPGA2**	**FPGA3**	**FPGA4**
PATCH1	AE19	AB20	W19	M18
PATCH2	AF19	AC20	Y19	L18
PATCH3	M20	AE21	AB23	Y21
PATCH4	L20	AF21	AC23	AA21
SIGNAL NAME	**RIGHT TOP ROW**			
	FPGA1	**FPGA2**	**FPGA3**	**FPGA4**
PATCH1	F9	B6	M10	H7
PATCH2	E9	A6	L10	G7
PATCH3	D8	B7	J8	F6
PATCH4	C8	A7	H8	E6
SIGNAL NAME	**RIGHT CENTRE ROW**			
	FPGA1	**FPGA2**	**FPGA3**	**FPGA4**
PATCH1	M15	H15	F13	F11
PATCH2	K15	G15	E13	E11
PATCH3	L11	J14	G12	G10
PATCH4	K11	H14	F12	F10

SIGNAL NAME	RIGHT BOTTOM ROW			
	FPGA1	FPGA2	FPGA3	FPGA4
PATCH1	F21	F19	J18	F17
PATCH2	E21	E19	H18	E17
PATCH3	K19	H21	M19	H19
PATCH4	J19	G21	L19	G19

3 Between Communications FPGA and Array FPGAs

Fig 1 above shows the 20 connections between the communications FPGA and each row of 4 FPGAs. These interconnections are shown below.

Connections between the Communications FPGA and the Left Array:

SIGNAL NUMBER	LEFT TOP ROW		LEFT CENTRE ROW		LEFT BOTTOM ROW	
	COMMS FPGA PIN	ARRAY FPGA PIN	COMMS FPGA PIN	ARRAY FPGA PIN	COMMS FPGA PIN	ARRAY FPGA PIN
1	W17	C17	AA16	C17	W10	C17
2	Y18	A17	AB16	A17	Y10	A17
3	AA18	B16	Y15	B16	AA10	B16
4	AB18	A16	AB15	A16	AB10	A16
5	Y17	C15	W14	C15	Y9	C15
6	AB17	A15	Y14	A15	AB9	A15
7	V17	B14	Y13	B14	W9	B14
8	W18	A14	AB13	A14	Y8	A14
9	AA14	H11	T15	H11	AA6	H11
10	AB14	G11	U15	G11	AB6	G11
11	U16	B12	W12	B12	Y7	B12
12	V15	A12	Y12	A12	AB7	A12
13	V13	D10	Y11	D10	Y5	D10
14	W13	C10	AB11	C10	AB5	C10
15	U14	D9	V11	D9	AA4	D9
16	U13	D8	W11	D8	AB4	D8
17	Y16	C13	AA12	C13	AA8	C13
18	W15	A13	AB12	A13	AB8	A13
19	AA2	C7	T12	C7	W6	C7
20	AA1	A7	U12	A7	Y6	A7

Connections between the Communications FPGA and the Right Array:

SIGNAL NUMBER	RIGHT TOP ROW		RIGHT CENTRE ROW		RIGHT BOTTOM ROW	
	COMMS FPGA PIN	ARRAY FPGA PIN	COMMS FPGA PIN	ARRAY FPGA PIN	COMMS FPGA PIN	ARRAY FPGA PIN
1	B3	AB18	D18	AB18	H13	AB18
2	A3	AA18	D19	AA18	G13	AA18
3	B2	AA16	B20	AA16	H12	AA16
4	A2	AB16	A20	AB16	G11	AB16
5	F2	Y15	C19	Y15	H10	Y15
6	F1	AB15	A19	AB15	H11	AB15
7	R11	AA14	B18	AA14	G9	AA14
8	T11	AB14	A18	AB14	F10	AB14

9	T8	W14	G16	W14	E5	W14
10	U8	Y14	F17	Y14	E6	Y14
11	R9	W12	D17	W12	F7	W12
12	R8	Y12	C18	Y12	F8	Y12
13	T7	W11	E16	W11	C5	W11
14	U6	Y10	F16	Y10	A5	Y10
15	U9	AA10	F14	AA10	D4	AA10
16	V9	AB10	F15	AB10	D5	AB10
17	T10	Y13	C17	Y13	G8	Y13
18	U10	AB13	A17	AB13	F9	AB13
19	V7	W9	H14	W9	C4	W9
20	W8	Y8	G15	Y8	A4	Y8

4 Between Adjacent Array FPGAs

Each FPGA connects to its neighbours above, below and to each side (except where a device connects to DDR3 instead). There are 38 connections from each FPGA to its right/left neighbour (20 if LX45/LX75 devices are fitted) which are connected as pairs of signals on 3.3V IO banks.

LEFT		RIGHT	
SIGNAL NAME	**PIN**	**SIGNAL NAME**	**PIN**
LBUS1	C17	RBUS1	AB18
LBUS2	A17	RBUS2	AA18
LBUS3	B16	RBUS3	AA16
LBUS4	A16	RBUS4	AB16
LBUS5	C15	RBUS5	Y15
LBUS6	A15	RBUS6	AB15
LBUS7	B14	RBUS7	AA14
LBUS8	A14	RBUS8	AB14
LBUS9	H11	RBUS9	W14
LBUS10	G11	RBUS10	Y14
LBUS11	B12	RBUS11	W12
LBUS12	A12	RBUS12	Y12
LBUS13	D10	RBUS13	W11
LBUS14	C10	RBUS14	Y10
LBUS15	D9	RBUS15	AA10
LBUS16	D8	RBUS16	AB10
LBUS17	C13	RBUS17	Y13
LBUS18	A13	RBUS18	AB13
LBUS19	C7	RBUS19	W9
LBUS20	A7	RBUS20	Y8
LBUS21	F10	RBUS21	R13
LBUS22	E10	RBUS22	U13
LBUS23	D15	RBUS23	T14
LBUS24	C14	RBUS24	U14
LBUS25	C5	RBUS25	Y7
LBUS26	A5	RBUS26	AB7
LBUS27	C9	RBUS27	T12
LBUS28	A9	RBUS28	U12

LBUS29	B6	RBUS29	T10
LBUS30	A6	RBUS30	U10
LBUS31	D7	RBUS31	U9
LBUS32	C8	RBUS32	V9
LBUS33	B8	RBUS33	V11
LBUS34	A8	RBUS34	W10
LBUS35	D6	RBUS35	V7
LBUS36	C6	RBUS36	W8
LBUS37	D13	RBUS37	R11
LBUS38	D12	RBUS38	T11

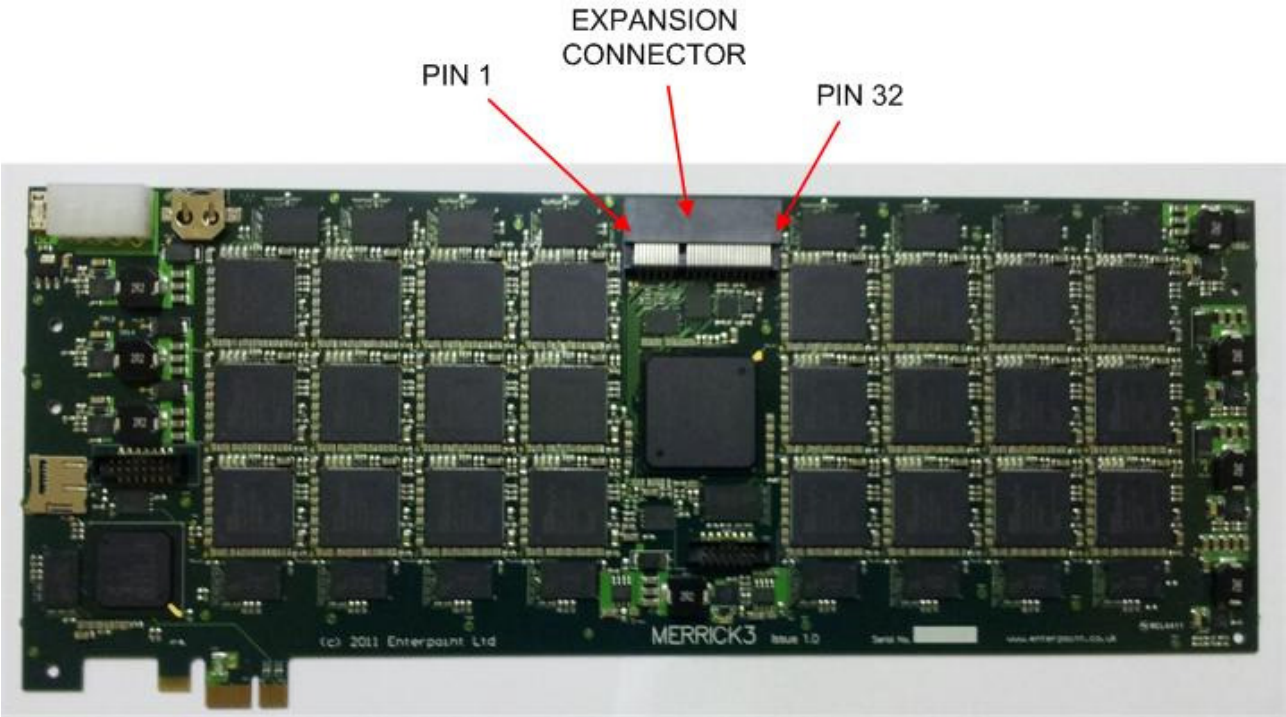
Signals shown in yellow are not connected on LX75 or LX45 FPGA sizes

There are 80 connections from each FPGA to its neighbour above/below (except where DDR3 is fitted) which are connected as pairs of signals on 1.5V IO banks.

UP		DOWN	
SIGNAL NAME	**PIN**	**SIGNAL NAME**	**PIN**
UBUS1	L20	DBUS1	L3
UBUS2	L22	DBUS2	L1
UBUS3	J17	DBUS3	K2
UBUS4	J19	DBUS4	K1
UBUS5	M18	DBUS5	M2
UBUS6	M19	DBUS6	M1
UBUS7	N19	DBUS7	P6
UBUS8	M20	DBUS8	P5
UBUS9	N20	DBUS9	N3
UBUS10	N22	DBUS10	N1
UBUS11	P21	DBUS11	P2
UBUS12	P22	DBUS12	P1
UBUS13	R20	DBUS13	R3
UBUS14	R22	DBUS14	R1
UBUS15	T21	DBUS15	T2
UBUS16	T22	DBUS16	T1
UBUS17	U20	DBUS17	U3
UBUS18	U22	DBUS18	U1
UBUS19	V21	DBUS19	V2
UBUS20	V22	DBUS20	V1
UBUS21	P17	DBUS21	W3
UBUS22	P18	DBUS22	W1
UBUS23	AA21	DBUS23	U8
UBUS24	AA22	DBUS24	T7
UBUS25	Y21	DBUS25	Y2
UBUS26	Y22	DBUS26	Y1
UBUS27	AA20	DBUS27	Y3
UBUS28	AB21	DBUS28	AB3
UBUS29	R17	DBUS29	U6
UBUS30	R19	DBUS30	V5
UBUS31	T19	DBUS31	T4
UBUS32	T20	DBUS32	T3

UBUS33	D19	DBUS33	G6
UBUS34	D20	DBUS34	G4
UBUS35	C18	DBUS35	E4
UBUS36	C19	DBUS36	F3
UBUS37	G17	DBUS37	N7
UBUS38	G19	DBUS38	N6
UBUS39	B20	DBUS39	C4
UBUS40	A21	DBUS40	D3
UBUS41	F17	DBUS41	4
UBUS42	F18	DBUS42	H3
UBUS43	A19	DBUS43	B2
UBUS44	A20	DBUS44	B1
UBUS45	H17	DBUS45	K6
UBUS46	H18	DBUS46	K5
UBUS47	F19	DBUS47	J6
UBUS48	F20	DBUS48	J4
UBUS49	V19	DBUS49	U4
UBUS50	V20	DBUS50	V3
UBUS51	L19	DBUS51	M5
UBUS52	K20	DBUS52	L4
UBUS53	Y19	DBUS53	W4
UBUS54	Y20	DBUS54	Y4
UBUS55	F21	DBUS55	G3
UBUS56	F22	DBUS56	G1
UBUS57	H19	DBUS57	P4
UBUS58	H20	DBUS58	R4
UBUS59	E20	DBUS59	F2
UBUS60	E21	DBUS60	F1
UBUS61	G20	DBUS61	H2
UBUS62	G22	DBUS62	H1
UBUS63	D21	DBUS63	E3
UBUS64	D22	DBUS64	E1
UBUS65	H21	DBUS65	J3
UBUS66	H22	DBUS66	J1
UBUS67	C20	DBUS67	D2
UBUS68	C22	DBUS68	D1
UBUS69	K18	DBUS69	K4
UBUS70	K19	DBUS70	K3
UBUS71	B21	DBUS71	C3
UBUS72	B22	DBUS72	C1
UBUS73	P19	DBUS73	T6
UBUS74	P20	DBUS74	T5
UBUS75	J21	DBUS75	N4
UBUS76	J22	DBUS76	P3
UBUS77	AB19	DBUS77	AA4
UBUS78	AB20	DBUS78	AA3
UBUS79	M16	DBUS79	M4
UBUS80	M17	DBUS80	M3

5. Between the Control FPGA and the Expansion connector



Merrick3 has an expansion connector (Samtec type PCIE-064-02-F-D-RA) which is connected to the Control FPGA via its MGT interface to allow stacking of Merrick3 boards and expansion to other compatible boards using a PCIE interface. The connections are shown below:

CONNECTOR PIN	SIGNAL	CONTROL FPGA PIN		CONNECTOR PIN	SIGNAL	CONTROL FPGA PIN
A1	PRESENCE			B1	NC	
A2	NC			B2	NC	
A3	NC			B3	NC	
A4	GND			B4	GND	
A5	NC			B5	NC	
A6	NC			B6	NC	
A7	NC			B7	GND	
A8	NC			B8	NC	
A9	NC			B9	NC	
A10	NC			B10	NC	
A11	PCIE_PWRGD_P	AE3		B11	NC	
A12	GND			B12	NC	
A13	REFCLK_P	AJ13		B13	GND	
A14	REFCLK_N	AK13		B14	RX0_P	AG10
A15	GND			B15	RX0_N	AH10
A16	TX0_P	AJ9		B16	GND	
A17	TX0_N	AK9		B17	PRESENCE	
A18	GND			B18	GND	

A19	NC			B19	RX1_P	AG12
A20	GND			B20	RX1_N	AH12
A21	TX1_P	AJ11		B21	GND	
A22	TX1_N	AK11		B22	GND	
A23	GND			B23	RX2_P	AG20
A24	GND			B24	RX2_N	AH20
A25	TX2_P	AJ21		B25	GND	
A26	TX2_N	AK21		B26	GND	
A27	GND			B27	RX3_P	AG22
A28	GND			B28	RX3_N	AH22
A29	TX3_P	AJ23		B29	GND	
A30	TX3_N	AK23		B30	NC	
A31	GND			B31	PRESENCE	
A32	NC			B32	GND	

Pins marked NC are not connected. The three PRESENCE pins are connected only to each other

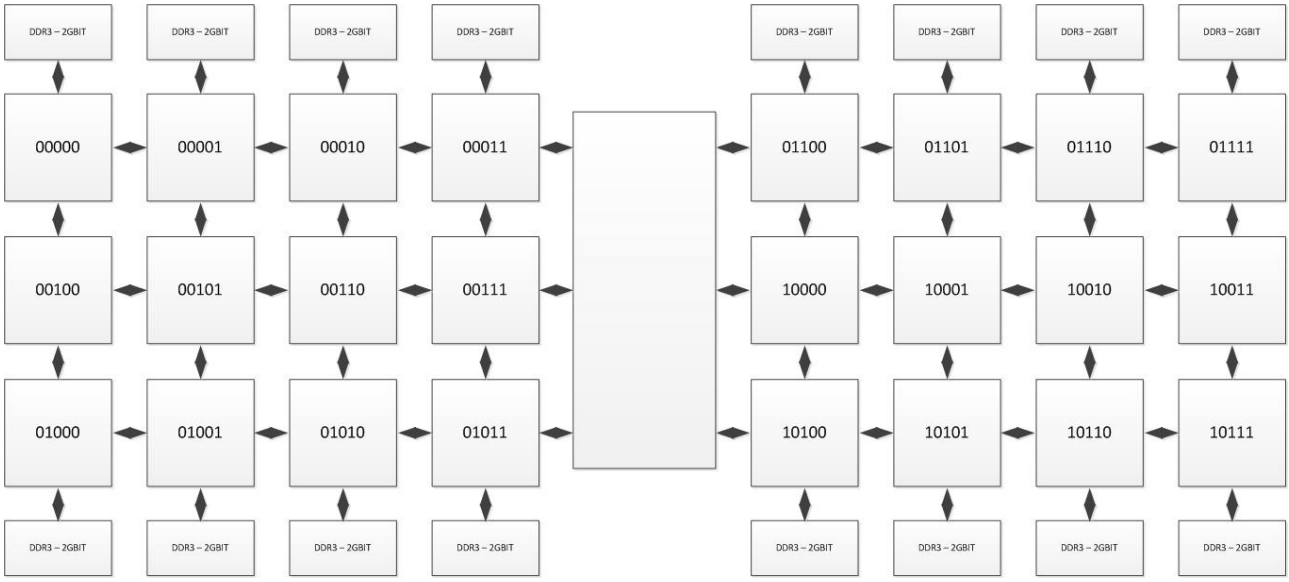
.

DEVICE ID CODES

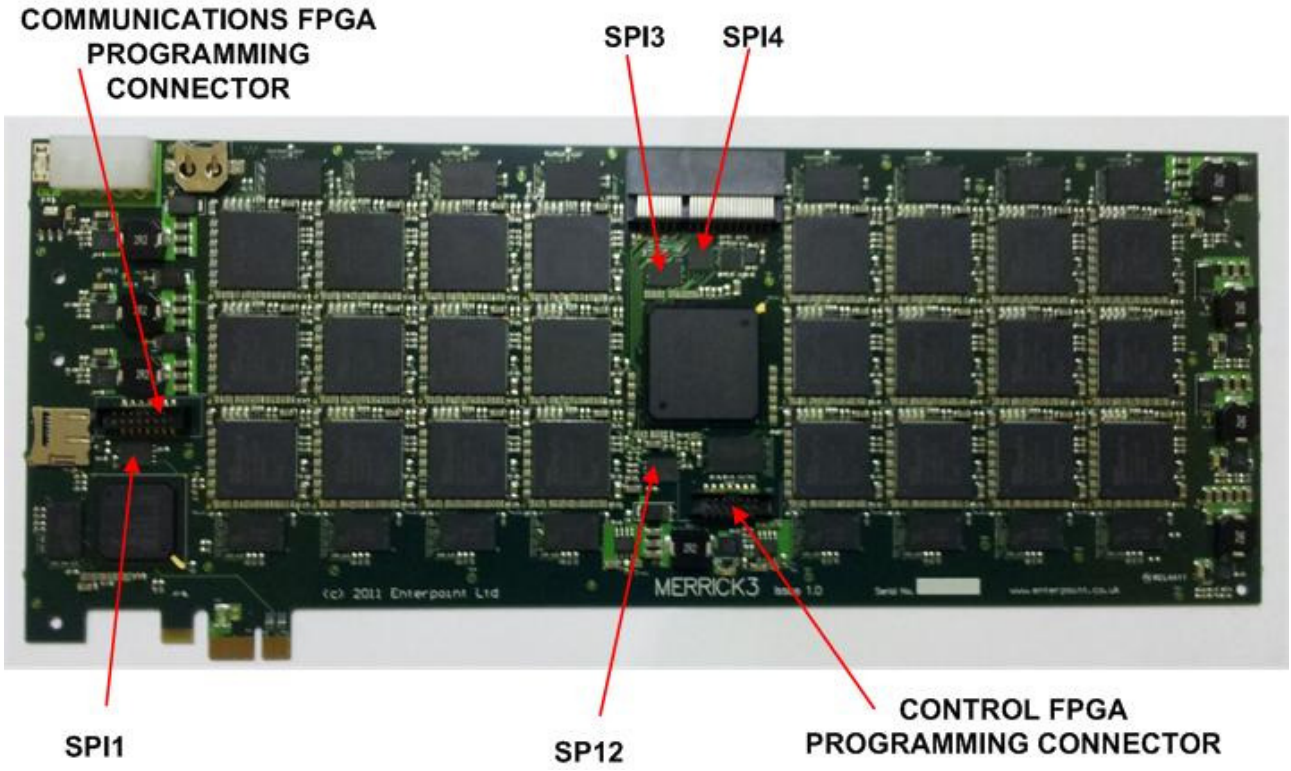
Each of the 24 Array FPGAs has a unique 5-bit ID code accessed on the following pins:

ID CODE BIT	TOP ROW	CENTRE/BOTTOM ROW
ID1	Y20	H16
ID2	R15	H13
ID3	R16	H14
ID4	R17	L15
ID5	R19	J16

The ID codes of each device can be seen on the PCB plan below:



SPI FLASH MEMORY



There are 4 SPI flash memory devices fitted to Merrick3. One is connected to the Communications FPGA for configuration code. A second is connected to the Control FPGA for configuration code. The third and fourth devices are connected to the Control FPGA for extra code storage. The details of these devices are shown below.

1. The W25Q128BV SPI flash memory device SPI1 configures the Communications FPGA when it is powered providing a suitable bitstream is programmed into the device. The W25Q128BV has a capacity of 128Mbits with a single configuration bitstream for the XC6SLX45T taking 1.45Mbits. Any remaining space can be used for alternative configurations or code and data storage. The W25Q128BV is a quad flash device, and with suitably chosen configuration options will allow the Merrick board to achieve the 100ms minimum PCIE configuration time.

After configuration the SPI Flash can be accessed via the following pins of the FPGA:

SIGNAL	FPGA PIN	W25Q128BV PIN
CCLK	Y20	6
MISO0/D	AB20	5
MISO1/Q	AA20	2
MISO2/WP	R13	3
MISO3/HOLD	T14	7
CS	AA3	1

The flash memory can be programmed using direct SPI programming from the Communications FPGA programming connector.

2. The W25Q128BV SPI flash memory device SPI2 configures the Control FPGA when it is powered providing a suitable bitstream is programmed into the device. The W25Q128BV has a capacity of 128Mbits with a single configuration bitstream for the XC6SLX150T taking 4.1Mbits . Any remaining space can be used for alternative configurations or code and data storage. Although this W25Q128BV is capable of being used as a quad flash device, it is only available for x1 configuration.

After configuration the SPI Flash can be accessed via the following pins of the FPGA:

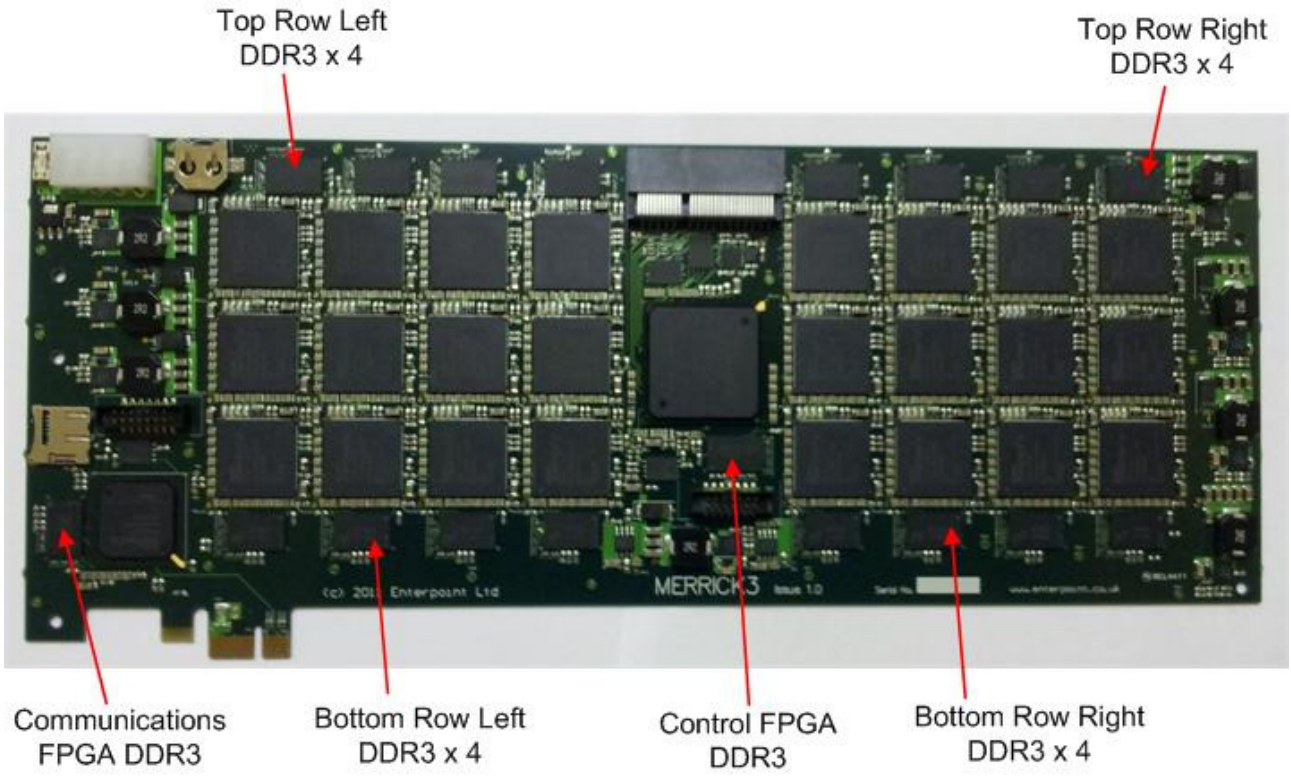
SIGNAL	FPGA PIN	W25Q128BV PIN
CCLK	AJ26	6
DIN	AJ25	2
MOSI	AK25	5
CSO_B	AK6	1

Pin 7 of this flash memory device (Hold) is permanently pulled up to 3.3V.
The flash memory can be programmed using direct SPI programming from the 7x2 Control FPGA Programming Connector. The WRITE Signal is connected to pin **W24** of the Control FPGA and also pulled up to 3.3V.

3 and 4. These W25Q128BV SPI flash memory devices SPI3 and SPI4 are available for user code and data storage. They are connected to GPIO on the Control FPGA and can be used in either x1 or x4 mode.
The SPI Flash devices can be accessed via the following pins of the FPGA:

SIGNAL	FPGA PIN SPI3	FPGA PIN SPI4	W25Q128BV PIN
CCLK	AH1	AF2	6
MISO0/D	AG1	AF1	5
MISO1/Q	AJ2	AD2	2
MISO2/WP	AJ1	AD1	3
MISO3/HOLD	AK2	AF3	7
CS	AH2	AE1	1

DDR3 MEMORY



Merrick3 has 18 2GBIT DDR3 Micron MT41J128M16LA device as standard, 16 connected to the Array FPGAs and one each connected to the Communications andControl FPGAs.. These devices are organised as 8 Meg x 32 x 8 banks. They are supported by the hard core memory controller that is in the Spartan-6 FPGAs. To add these cores to your design the COREGEN tool, part of the ISE suite, will generate implementation templates in VHDL or Verilog for the configuration that you want to use. More details on the memory controller can be found in the user guide. http://www.xilinx.com/support/documentation/user_guides/ug388.pdf.

The DDR3 devices have 14 address lines and 16 data lines to address all the available memory, which can be accessed at speeds of 1.87ns. More details of the DDR3 can be found in http://download.micron.com/pdf/datasheets/dram/ddr3/1Gb_DDR3_SDRAM.pdf.

For OEM applications we can fit bigger DDR3 parts subject to limitations of the memory controller.

The DDR3 sites have the following connections to the FPGAs:

DDR3 FUNCTION	Communications FPGA PIN	Control FPGA PIN	Array FPGA	
			UPPER ROW	LOWER ROW
DDR_A0	H21	D28	B21	M5
DDR_A1	H22	D30	B22	L4
DDR_A2	G22	C30	C22	K3
DDR_A3	J20	E29	J21	M4
DDR_A4	H20	F27	D22	K5

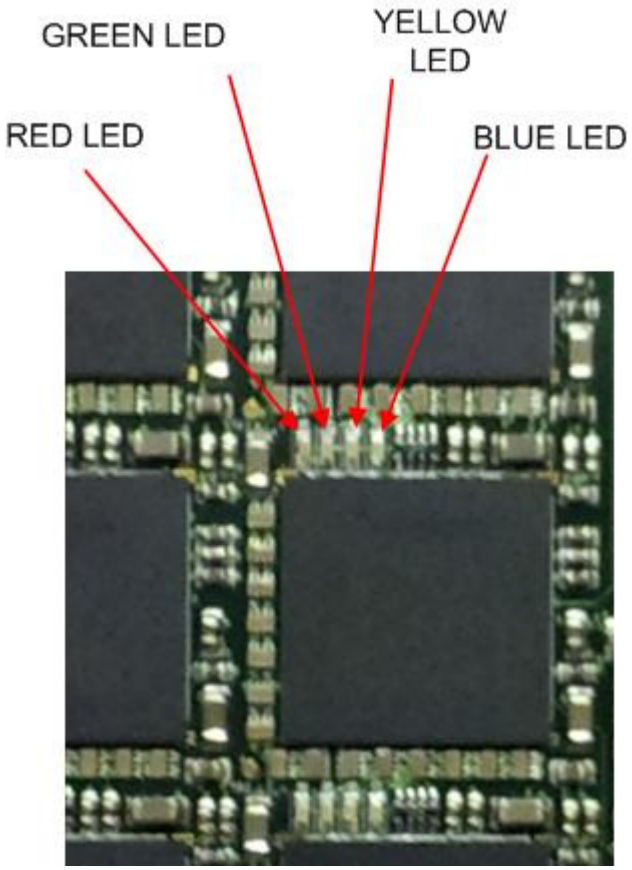
DDR_A5	M20	H26	L17	G3
DDR_A6	M19	H27	K17	G1
DDR_A7	G20	C29	C20	K4
DDR_A8	E20	B27	G20	C3
DDR_A9	E22	A27	G22	C1
DDR_A10	J19	F26	D21	K6
DDR_A11	H19	A26	H20	B1
DDR_A12	F22	B30	E22	J4
DDR_A13	G19	A28	F21	H4
DDR_A14	F20	A29	F22	H3
DDR_A15	F18	G25	F20	T3
DDR_BA0	K17	D27	K18	E3
DDR_BA1	L17	C27	K19	E1
DDR_BA2	K18	D26	H22	D1
DDR_CS_N	H17	L25	H18	H6
DDR_RAS_N	K21	K26	M18	N4
DDR_WE_N	K19	E26	H21	D2
DDR_DQ0	R20	H28	N20	N3
DDR_DQ1	R22	H30	N22	N1
DDR_DQ2	P21	G29	N19	M2
DDR_DQ3	P22	G30	M20	M1
DDR_DQ4	L20	G27	L20	J3
DDR_DQ5	L22	G28	L22	J1
DDR_DQ6	M21	F28	K21	K2
DDR_DQ7	M22	F30	K22	K1
DDR_DQ8	T21	L27	P21	P2
DDR_DQ9	22	L28	P22	P1
DDR_DQ10	U20	L29	R20	R3
DDR_DQ11	U22	L30	R22	R1
DDR_DQ12	W20	M26	U20	U3
DDR_DQ13	W22	M27	U22	U1
DDR_DQ14	Y21	M28	V21	V2
DDR_DQ15	Y22	M30	V22	V1
DDR_LDM	N19	J28	K20	H1
DDR_LDQS	N20	J29	M21	L3
DDR_LDQS_N	N22	J30	M22	L1
DDR_UDM	P20	J27	L19	H2
DDR_UDQS	V21	K28	T21	T2
DDR_UDQS_N	V22	K30	T22	T1
DDR_ODT	J22	E30	J22	M3
DDR_CAS_N	K22	K27	M19	P3
DDR_RESET_N	H18	C26	H19	B2
DDR_CKE	F21	B29	E20	J6
DDR_CLK_N	L19	E28	J19	F1
DDR_CLK	K20	E27	J17	F2
NOCONNECT*	L15	N24	AA22	R9
TERMINATION*	B22	L24	AB20	Y1
TIMING LOOP**	NONE	NONE	N15-N16	K7-K8

The signals shown shaded in yellow are terminated using suitable arrangements of resistors.

* The Noconnect and Termination pins are required when building some versions of the memory controller core. Note: ISE Version 13 and above permit greater flexibility when assigning these pins than earlier ISE versions.

**Timing loops have been implemented for the Array FPGAs to facilitate compensation for temperature and timing delays where necessary.

LEDS



Merrick3 has a total of 96 LEDs. Each array FPGA has one each of Red, Yellow, Blue and Green LEDs.

The relevant IO pin for an LED needs to be asserted low to ensure the specified LED turns on. It may be necessary to assign the pins to 'Z' (High Impedance) in order for the LEDs to be completely 'off'.

The table below shows the connections between the FPGAs and the LEDs.

COLOUR	FPGA PIN	
	UPPER ROW	CENTRE AND LOWER ROWS
RED	AA20	K22
GREEN	AA21	M21
BLUE	M17	L17
YELLOW	Y22	M22

PCIE INTERFACE

Merrick3 has a x1 PCIe Interface connected between the PCIE edge connector and the Communications FPGA. The pin out of the Communications FPGA has been chosen such that the PCI interface follows the pinout for the XilinxTM SpartanTM-6 hard core for PCIe which can be generated automatically by the XilinxTM Core Generator.
The connections between the PCIe connector and the FPGA are shown below.

SIGNAL NAME	PCIE CONNECTOR PIN	FPGA PIN
PCIE_CLK_P	A13	A10
PCIE_CLK_N	A14	B10
PCIE_TX_P	A16	B6
PCIE_TX_N	A17	A6
PCIE_RX_P	B14	D7
PCIE_RX_P	B15	C7
PCIE_PRESENT#1	A1	
PCIE_PRESENT#2	B17	
PCIE_PWRGD	A11	D3

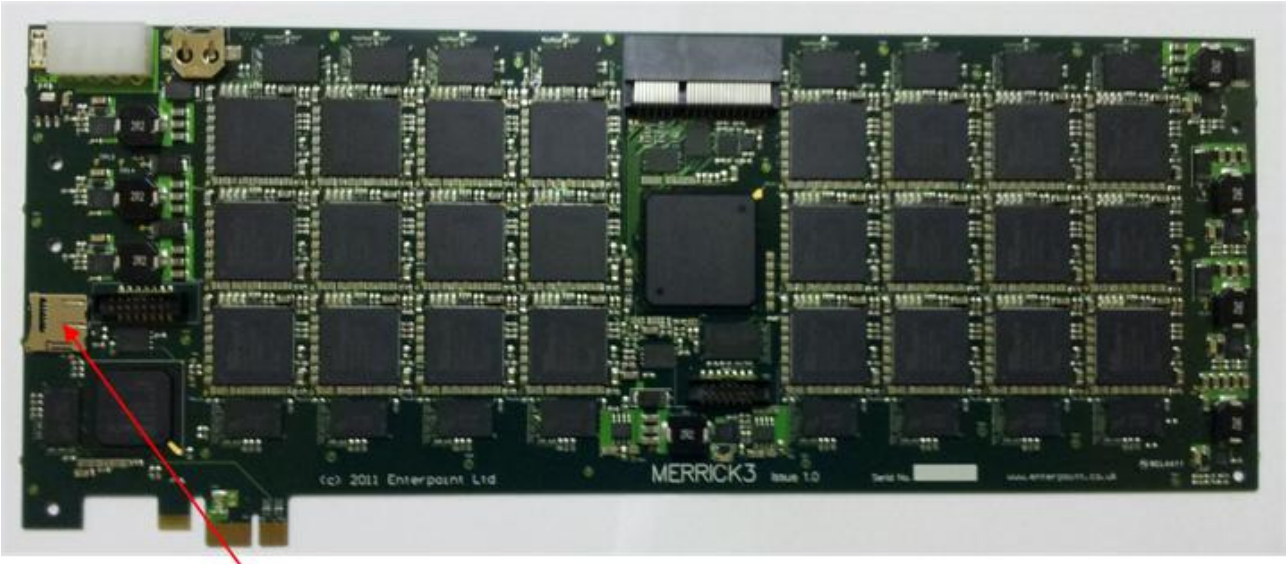
The two PCIE PRESENT signals are connected to each other.

Battery backup – location,

The Merrick3 has a battery holder which is available to provide battery backup to the FPGA. It is connected to the Spartan™-6 devices on the pins shown below. The battery holder accepts a 3V Lithium battery size CR1220 or equivalent.

DEVICE	BATTERY CONNECTION
Communications FPGA	n/c
Control FPGA	AB26
Array FPGAs	U17

MICRO SD CARD HOLDER



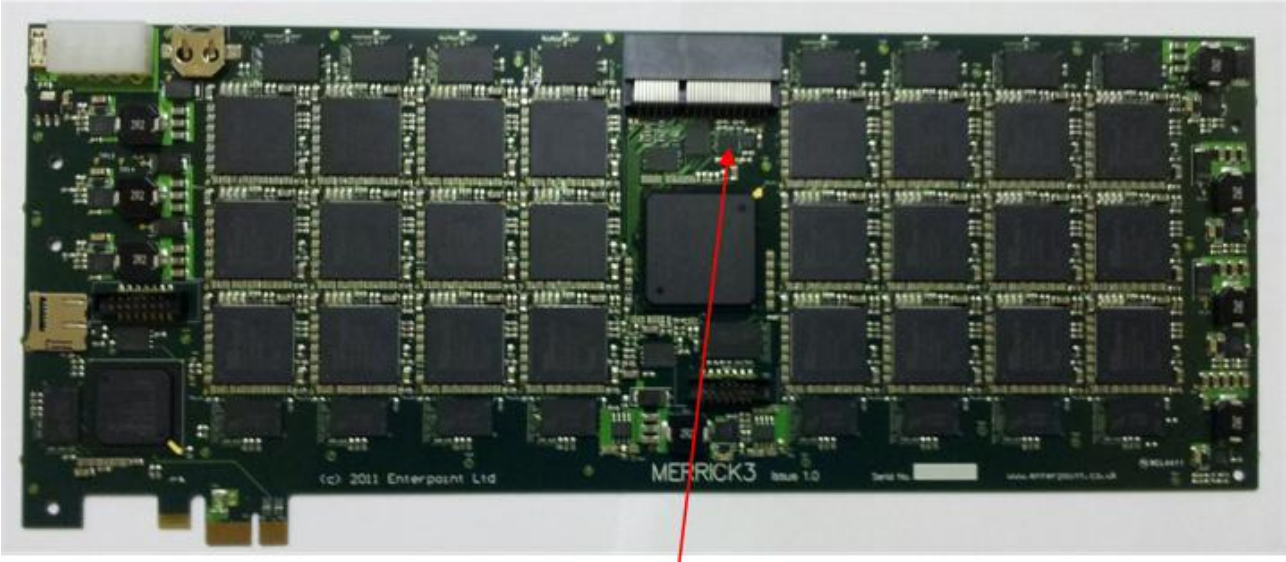
Further access to data can be achieved using the Micro SD Card Socket which is connected to the Communications FPGA. To use this socket in a design you may need to obtain a license from the SD Association at http://www.sdcard.org/home/.

The connections between the Micro SD Card Socket and the FPGA are shown below:

SDCARD SOCKET	SIGNAL NAME	FPGA PIN
DATA 1	MCARD1	P8
DATA 0	MCARD2	P7
DATA 2	MCARD3	N6
DATA 3	MCARD4	M7
CMD	MCARD5	N7
CLK	MCARD6	M8
POWER_ON_N	MCARD7	P6

The POWER_ON_N pin must be set LOW for power to be supplied to the SDCARD Reader.

CLOCK GENERATOR



MERRICK3 CLOCK GENERATOR

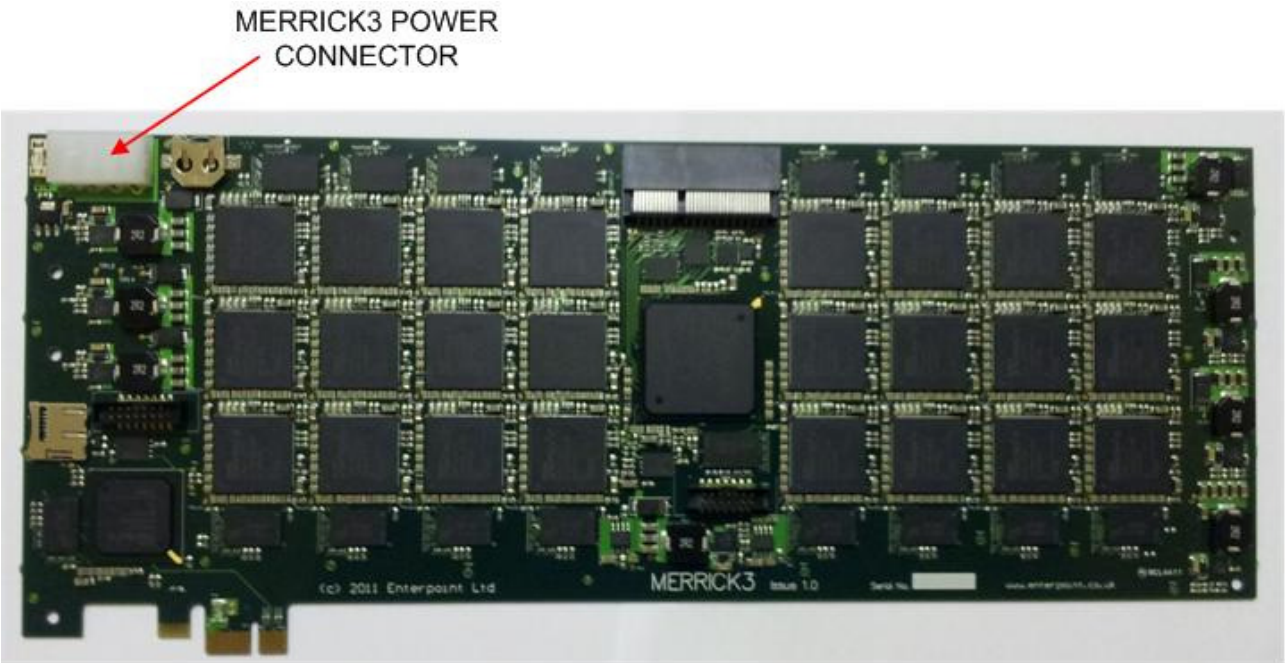
Merrick3 has an IDT5V19EE901NLGI clock generator capable of generating four single ended clocks and one differential clock which are all connected to FPGA. It can be used to generate clock frequencies in the range 4.9KHz to 500MHz. The clock generator is controlled by an I2C serial interface and has an internal EEPROM for storage of configuration data. Information and configuration software for this device are available from www.idt.com.

The connections between the Clock Generator and the FPGA are shown below:

SIGNAL NAME	IDT5V19EE901 FUNCTION	IDT5V19EE901 PIN	FPGA PIN
CLOCKGEN_BUS1	CLK_X	30	AA3
CLOCKGEN_BUS2	CLKA	7	AA1
CLOCKGEN_BUS3	CLKB	8	AB1
CLOCKGEN_BUS4	CLK C	24	AB2
CLOCKGEN_BUS5	P+ CLK (Differential Clock +ve)	10	W5
CLOCKGEN_BUS6	P-CLK (Differential Clock –ve)	11	W4
CLOCKGEN_BUS7	EXP_CLK1_P	14	V4
CLOCKGEN_BUS8	EXP_CLK1_N	15	V3
CLOCKGEN_BUS9	EXP_CLK2	23	U7
CLOCKGEN_BUS10	SDAT	18	V1
CLOCKGEN_BUS11	SCLK	19	U5

The Spartan-6 has Phase-Locked Loops and DCMs to produce multiples, divisions and phases of the clock for specific application requirements. Please consult the Spartan-6 datasheet available from the Xilinx website at http://www.xilinx.com if multiple clock signals are required.

POWER CONNECTIONS



Merrick3 is powered principally from the 12V supply on the disk drive connector. A limited 12V supply can be provided using the PCIE connector, but the current available is limited to 0.5A so this should be avoided unless you know that your design does not consume more current than this.

The Merrick3 is protected by 2 fuses. The 12v supply from the PCIE connector is protected by a 2.6A resettable fuse. The supply from the disk drive connector is protected by a 7A non-resettable fuse.

HEAT SINKS

Depending on the design implemented in the FPGAs on Merrick3, it will be necessary to implement a thermal dissipation scheme. One option is to add individual heatsinks to each FPGA e.g. those produced by Wakefield Thermal Solutions inc. (www.wakefield.com). Alternatively it may be necessary to attach fans to either the Merrick3 boards itself or to any enclosure used with Merrick3.

POWER REGULATORS

Merrick3 has 10 regulators supplying 3.3V, 1.5V, 1.2V and 0.75V power rails.

WARNING – REGULATORS CAN BECOME HOT IN NORMAL OPERATION ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THESE DEVICES WHILST THE MERRICK3 BOARD IS IN OPERATION.

Six Micrel MIC26950 regulators (REG 1 to 6) supply 1.2V with a maximum current available of 12A. These provide the core voltage for the FPGAs.

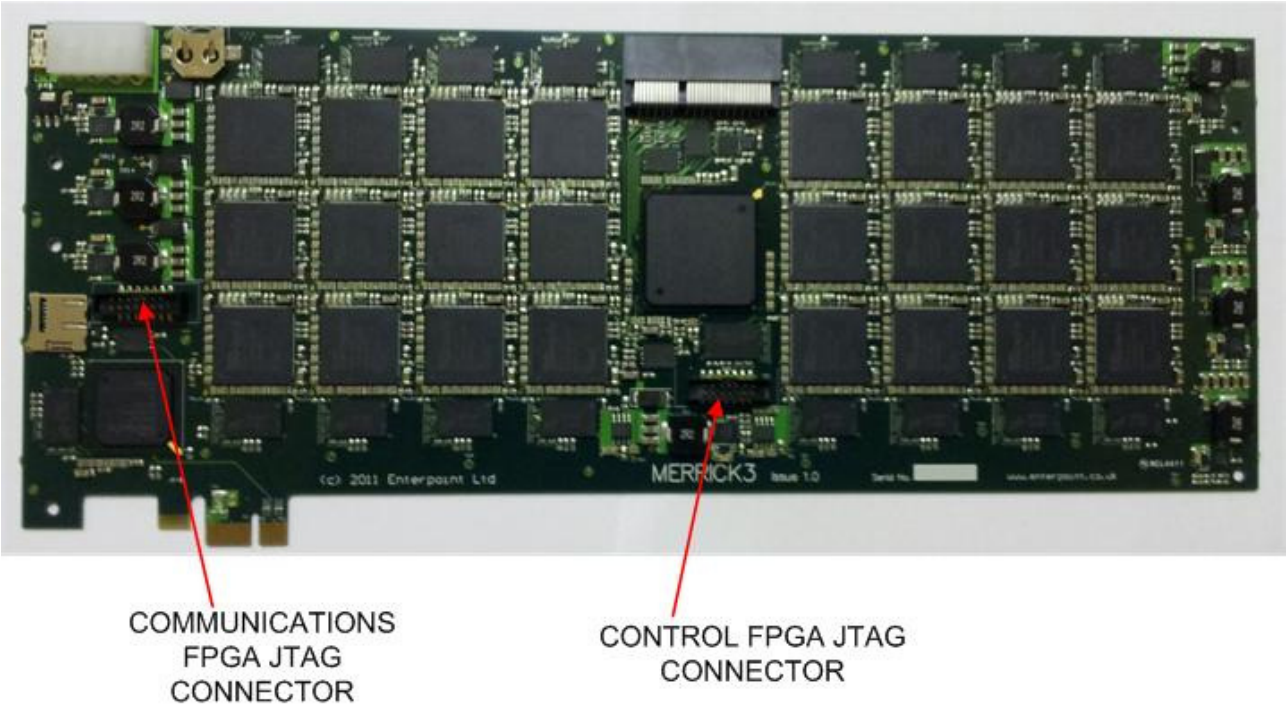
REGULATOR	SUPPLIES POWER TO
REG1	TOP LEFT ARRAY FPGAS
REG2	CENTRE LEFT ARRAY FPGAS
REG3	BOTTOM LEFT ARRAY AND COMMUNICATIONS FPGAS.
REG4	TOP RIGHT ARRAY AND CONTROL FPGAS.
REG5	CENTRE RIGHT ARRAY FPGAS
REG5	BOTTOM RIGHT ARRAY FPGAS

Another Micrel MIC26950 regulator (REG7) supplies 3.3V with a maximum current available of 12A. This is used for the some of the Array FPGA IOs, most of the Control and Communications FPGA IOs , the SDcard socket, the SPI Flash memories and the Clock Generator .

Another Micrel MIC26950 regulator (REG8) supplies 1.5V with a maximum current of 12A for the DDR3 and related FPGA I/O.

Two National Semiconductor LP2996 push-pull regulators (REG9 AND 10)each produce up to 1.5A at 0.75V. These provide reference and termination voltages for the DDR3 memory and related FPGA I/O. REG9 provides 0.75V for the left side array and Communications FPGA memories, REG10 serves the right side array and Control FPGA memories.

Programming Merrick3



The programming of the FPGA and SPI Flash parts on Merrick3 is achieved using the JTAG interface. Principally it is anticipated that a JTAG connection will be used in conjunction with Xilinx ISE software. The Spartan-6 series needs to be programmed using ISE 11 or higher. Versions of ISE prior to 11 do not support Spartan-6. The full version of the Xilinx tools is required to program the XC6SLX150. The free Webpack version of ISE is sufficient to support the LX45 and LX75 sizes of the FPGAs.

There are two JTAG connectors on Merrick3. The first allows programming of the Communications FPGA. The second allows programming of the Control FPGA. It is anticipated that the Array FPGAs will be programmed under control of the Master FPGA using code stored either in the DDR3 attached to the Control FPGA, the SPI flash memory devices connected to the Control FPGA or the SDCARD. A 16-bit wide configuration bus is routed from the Control FPGA to each block of 4 Array FPGAs together with individual FPGA Chip Select signals. Mode pins M0 and M1 are routed to the Control FPGA as are INIT_B, PROG_B, DONE, RDWR_B and CCLK. It is envisaged that the Slave SelectMAP interface will be used for configuration, but other options are available using these signals. Further information concerning Spartan6 Configuration options is available in the Spartan6 FPGA Configuration User guide UG380, available from www.xilinx.com.

The Array JTAG connections are connected to the Control FPGA. Each block of 4 FPGAs is connected as a single JTAG chain, The TDI signal connects to the device

closest to the Control FPGA and the TDO signal connects from the device furthest from the Control FPGA. TDI-TDO links exist between the remaining FPGAs in each block. The TCK and TMS signals are 'daisy-chained' along each block. The connections to the Control FPGA are shown below:

SIGNAL	LEFT TOP ROW	LEFT CENTRE ROW	LEFT BOTTOM ROW	RIGHT TOP ROW	RIGHT CENTRE ROW	RIGHT BOTTOM ROW
TDO	W7	Y2	AG26	U6	E3	M23
TDI	W6	AH4	AG30	L5	J3	N7
TMS	Y6	AK4	AK28	P4	L7	P26
TCK	Y4	Y1	AH26	T7	B1	M24

The two JTAG connectors have a layout as follows (top view):

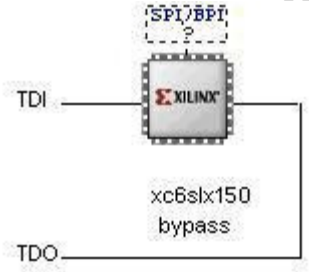
GND	GND	GND	GND	GND	GND	GND
NC	NC	TDI	TDO	TCK	TMS	3V3

The following procedure can be used to program the Communications and Control FPGAs

1. Programming an FPGA directly

Direct JTAG programming of the Spartan-6 FPGA is volatile and the FPGA will lose its configuration every time the board power is cycled. For sustained use of an FPGA design programming the design into the Flash memory is recommended (see 2 and 3 below).

Using iMPACT Boundary Scan the JTAG chain appears like this:

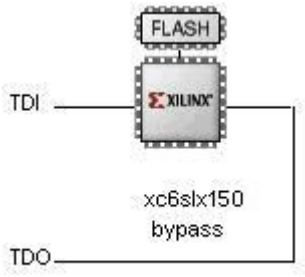


Direct JTAG programming using .bit files is useful for fast, temporary programming during development of FPGA programs. Right click the icon representing the Spartan-6 FPGA and choose 'Assign New Configuration File'. Navigate to your .bit file and choose 'OPEN'. The next dialogue box will offer to add a flash memory and you should decline. Right click the icon representing the Spartan-6 FPGA and choose 'Program'. On the next dialogue box ensure that the 'Verify' box is not checked. (If it is you should uncheck it, failure to do this will result in error messages being

displayed). Click OK. The Spartan-6 will program. This process is very quick (typically one second)

2. Programming the SPI flash memory using Boundary Scan.

Once the SPI Flash memory has been programmed, the Spartan-6 device will automatically load from the Flash memory at power up. Generation of suitable Flash memory files (.mcs) can be achieved using ISE iMPACT's Prom File Formatter.
To program the SPI flash right click on the icon representing the Spartan-6 and choose 'Add SPI/BPI Flash' Navigate to your programming file (.mcs) and click OPEN. Use the next dialogue box to select SPI flash and W25Q128BV. Data width should be set to 4(for the Communications FPGA) or 1 (for the Control FPGA). The flash memory should appear as shown below.



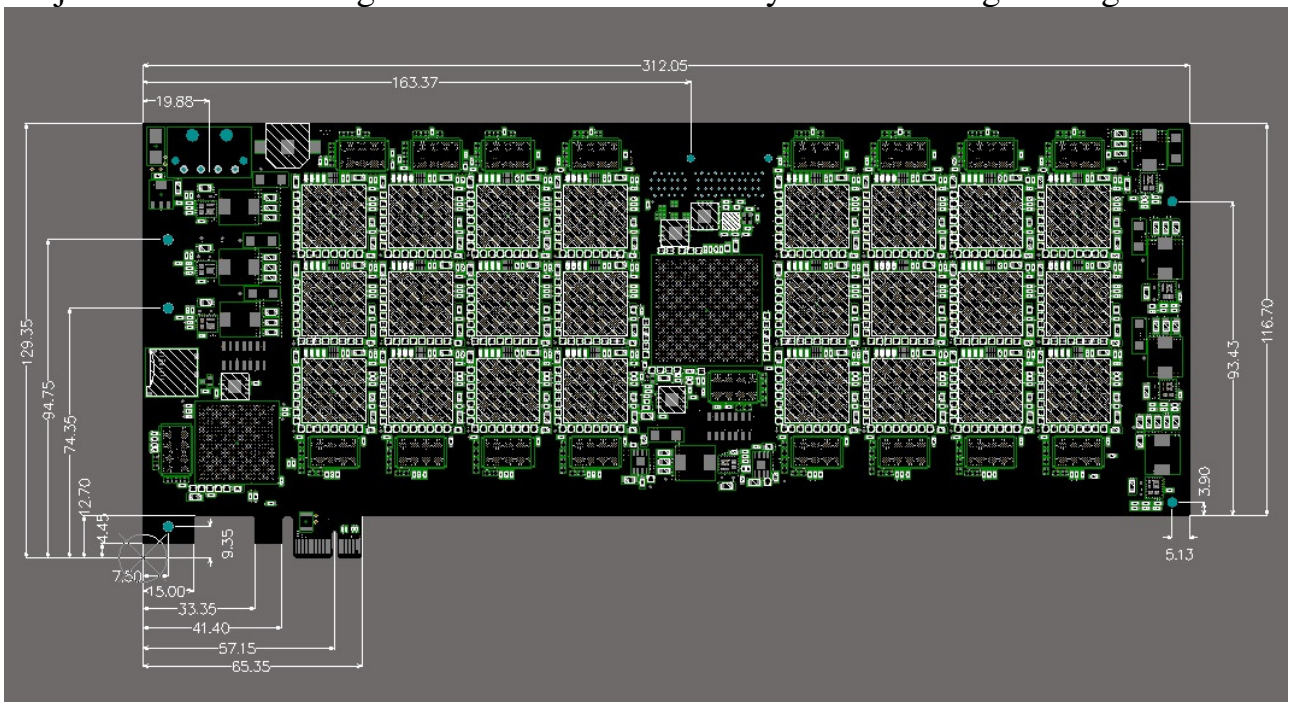
Right click on the icon representing the flash memory and choose 'Program' to load your program into the device. It is recommended that options to 'Verify' and 'Erase before programming' are chosen. Otherwise all defaults can be accepted. The programming operation will take some time (up to 10 minutes).

Depending upon the settings used when generating the bitfile using ISE, it will take up to 20 seconds for the XC6LX150 to configure upon power-up. In order to decrease this time the following process can be followed:

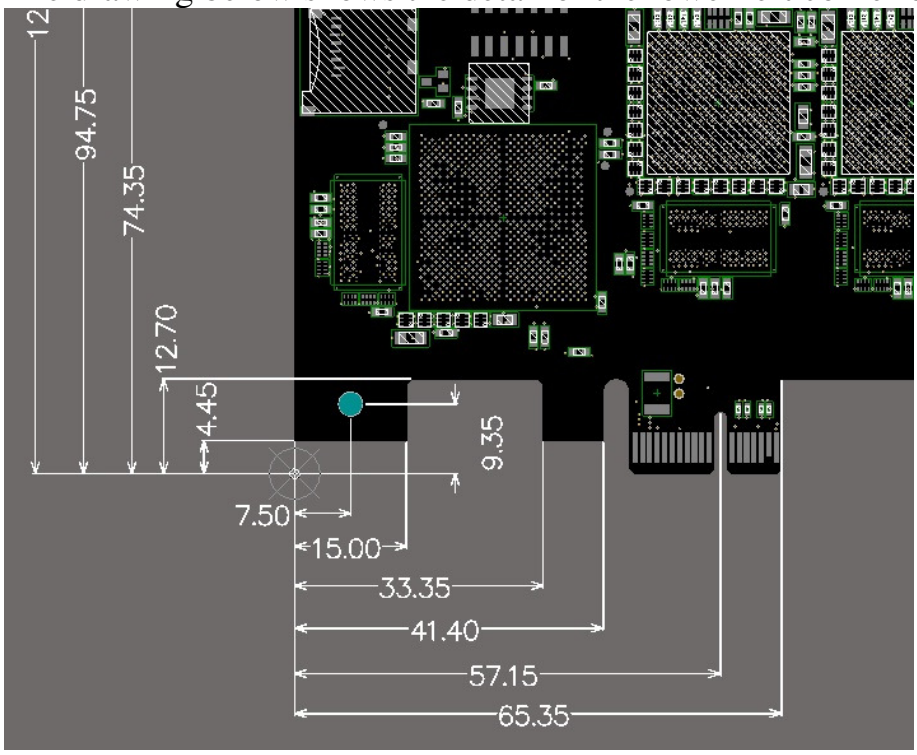
1. In the main ISE menu, right-click 'Generate Programming file'. Choose Properties.
2. On the left hand side of the Process Properties Dialogue box, choose Configuration Options.
3. The first item on the menu which appears on the right hand side of the dialogue box is 'Configuration Rate'. The default setting is 2. Increase this number. The maximum value we suggest is 22. Choose 'Apply' and 'OK'.
4. Generate the program file as normal.

MECHANICAL ARRANGEMENT

The Merrick3 PCB is a standard full-size PCIE PCB.
The Dimensions on the drawings below are millimetres (mm). All sizes quoted are subject to manufacturing tolerances and should only be used as a general guide.



The drawing below shows the detail of the lower left corner of the drawing above



The heights of the components, measured from the lower surface of the board are as follows:
Maximum height above PCB surface = 10mm approx (=height of expansion connector). The PCB is 1.6mm thick

Medical and Safety Critical Use

Merrick3 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accept no liability for any failure or defect of the Merrick3 board, or its design, when it is used in any medical or safety critical application.

Warranty

Merrick3 comes with a 90 day return to base warranty. Do not attempt to solder connections to the Merrick3. Enterpoint reserves the right not honour a warranty if the failure is due to soldering or other maltreatment of the Merrick3 board.

Outside warranty Enterpoint offers a fixed price repair or replacement service. We reserve the right not to offer this service where a Merrick3 has been maltreated or otherwise deliberately damaged. Please contact support if you need to use this service.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Please check our FAQ page for this product first before contacting support. FAQ is located at http://www.enterpoint.co.uk/drigmorn/Merrick3_faq.html. Telephone and email support is offered during normal United Kingdom working hours (GMT or GMT + 1) 9.00am to 5.00pm.

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